Design Challenges and Considerations of Wolfspeed 22kW High Efficiency Bi-directional ACDC Converter

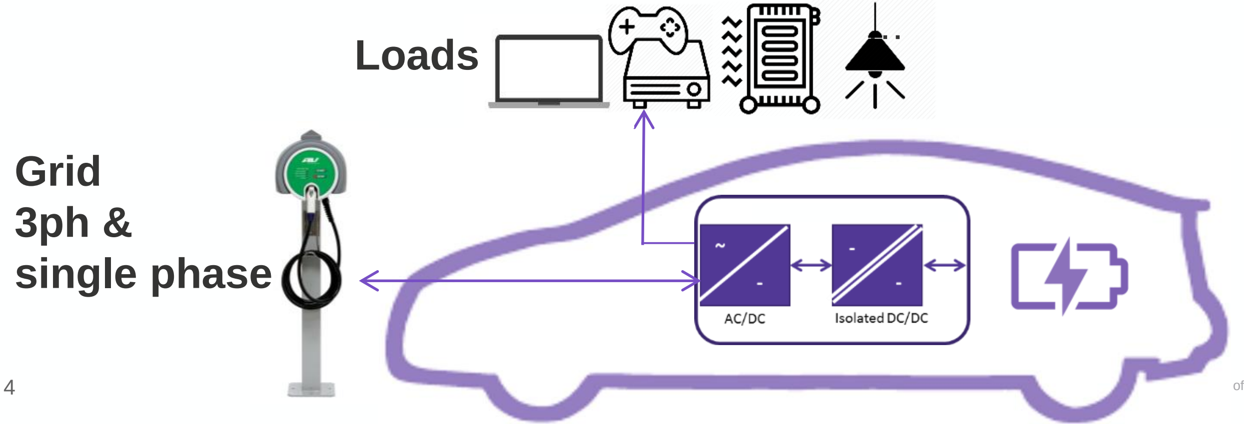
Jan 2021

Contents

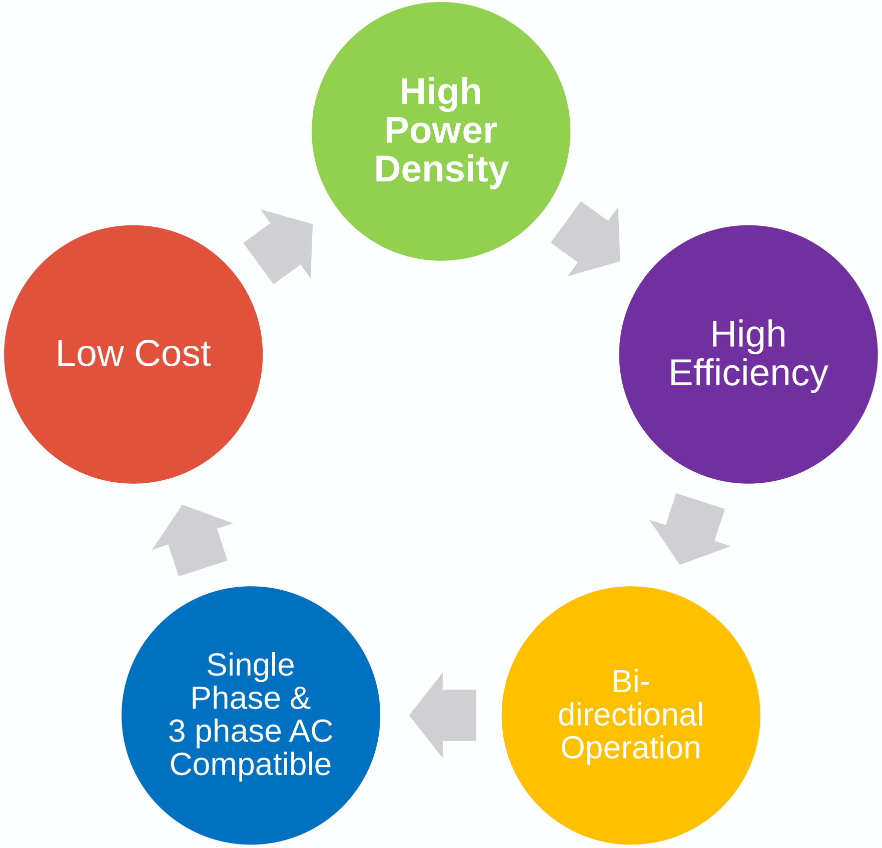
Specifications and Design Challenges

22kW Bi-Directional OBC Specifications

Description	3phase AC input Charging	1phase AC input Charging	Discharging Mode
Input Voltage	304Vac~456Vac	180Vac~264Vac	300Vdc-800Vdc
Output Voltage	200-800Vdc	200-800Vdc	220Vac
Rated Power	22kW 36A max	6.6kW	6.6kW
ACDC peak Efficiency	>98.5%	>98.5%	>98.5%
DCDC peak Efficiency	>98.5%	>98.5%	>98.5%
DC Bus Voltage	650V-900V	380V-900V	360V-760V

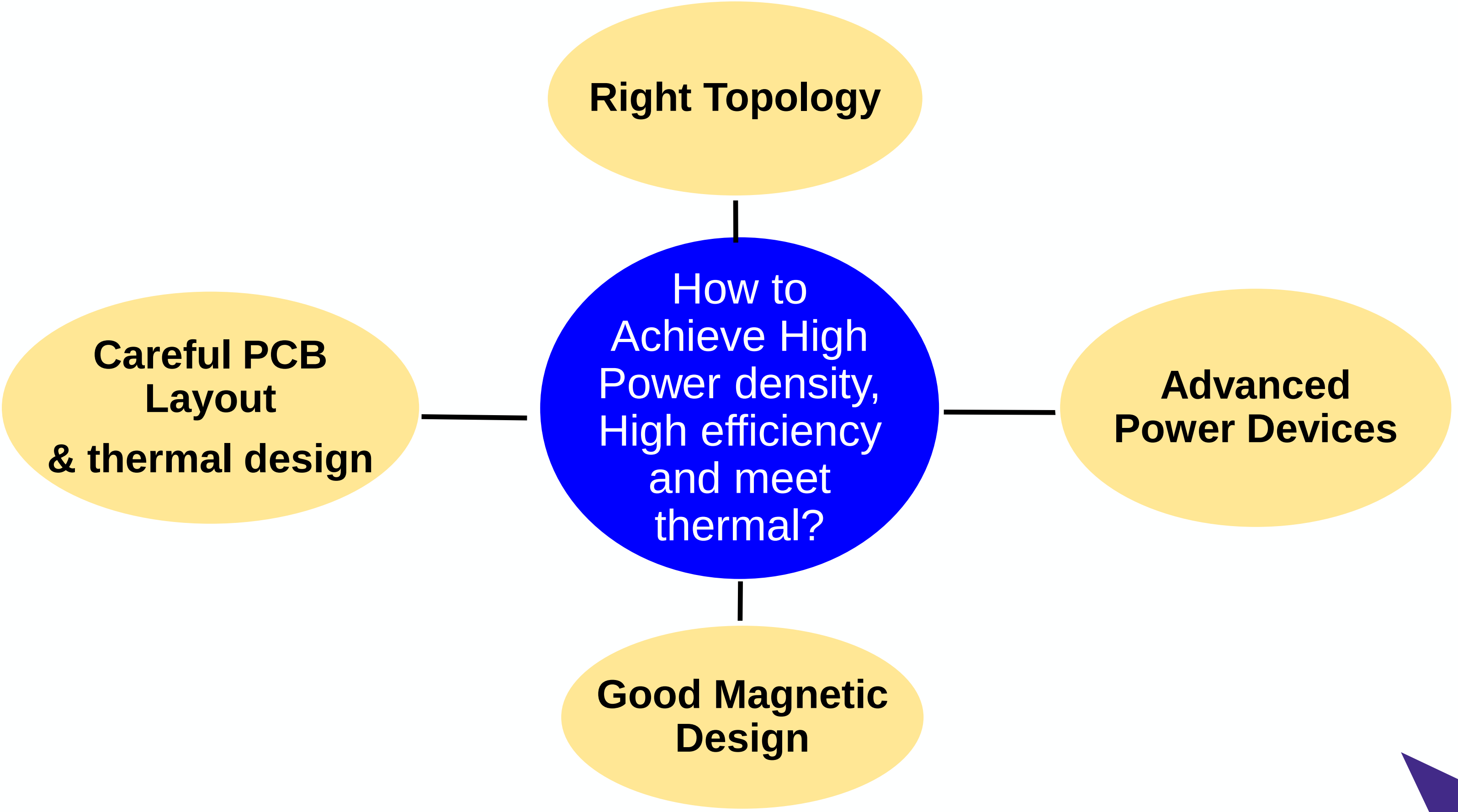


Design Trends and Challenges



- **How to achieve a high power density design?**
- **How to achieve high efficiency and meet thermal requirement?**
- **How to be compatible to both single phase and 3phases AC input?**
- **How to be cost-effective in Bi-directional application?**

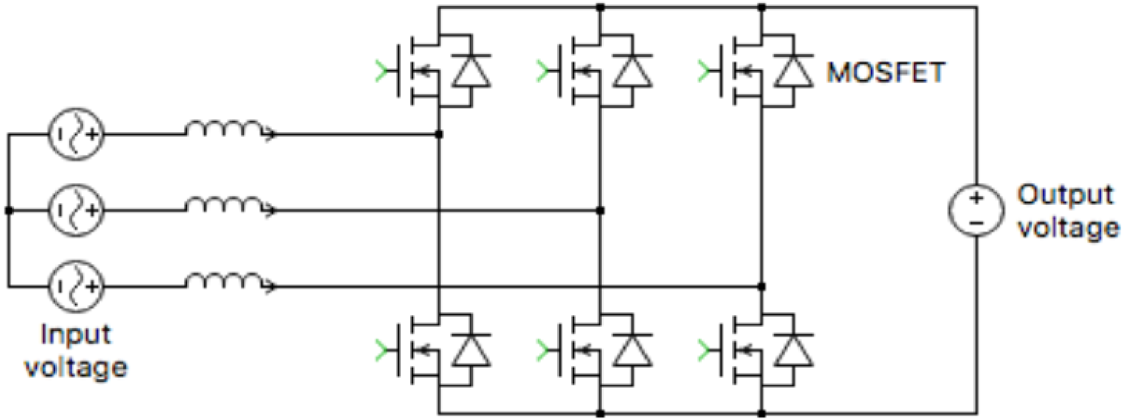
High Power Density, High Efficiency Design



Topology Selection for AC/DC

Candidate A for ACDC Converter

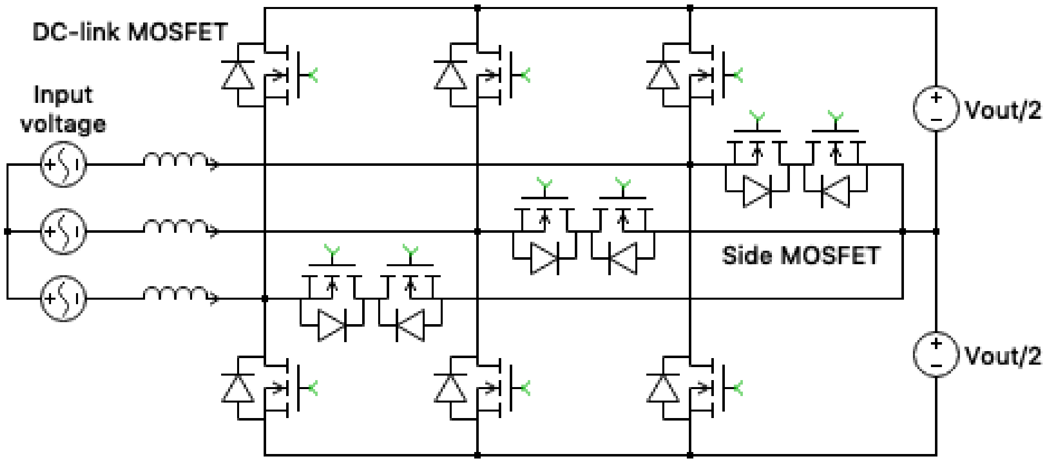
Six Switches Active Front End Converter



- ✓ Bi-directional Operation
- ✓ Low Parts Counts
- ✓ Simple Control/ Simple Drive/ Low Cost
- ✓ Single & 3 phase AC input Compatible

Candidate B for ACDC Converter

T-type ACDC Converter



- ✓ Bi-directional Operation
- ✓ Low Switching Loss/ Smaller Inductor
- ✓ Higher Parts Counts
- ✓ More Gate Drive/ Higher Cost

Topology Selection

Six Switches Active Front End Converter		T-type ACDC Converter	
Advantages	**Disadvantages**	**Advantages**	**Disadvantages**
Single & 3 phase AC input Compatible → Totem pole PFC with single phase AC input	Larger Choke	3level Converter → Lower switching loss, smaller choke, higher efficiency	More parts counts, → Larger Size, lower power density and higher cost
Lower parts counts, → Smaller Size, higher power density and lower cost	Hard switching 2 level converter → EMI concerns	3level → EMI friendly	Complex control for 6 DC-link MOSFETs + 6 Side MOSFETs
Easy to control at both 3ph and 1ph charging mode; also in discharging mode			

✓ For high Power Density and lower cost, Six Switches Active Front End Converter is selected.

Power Components Selection

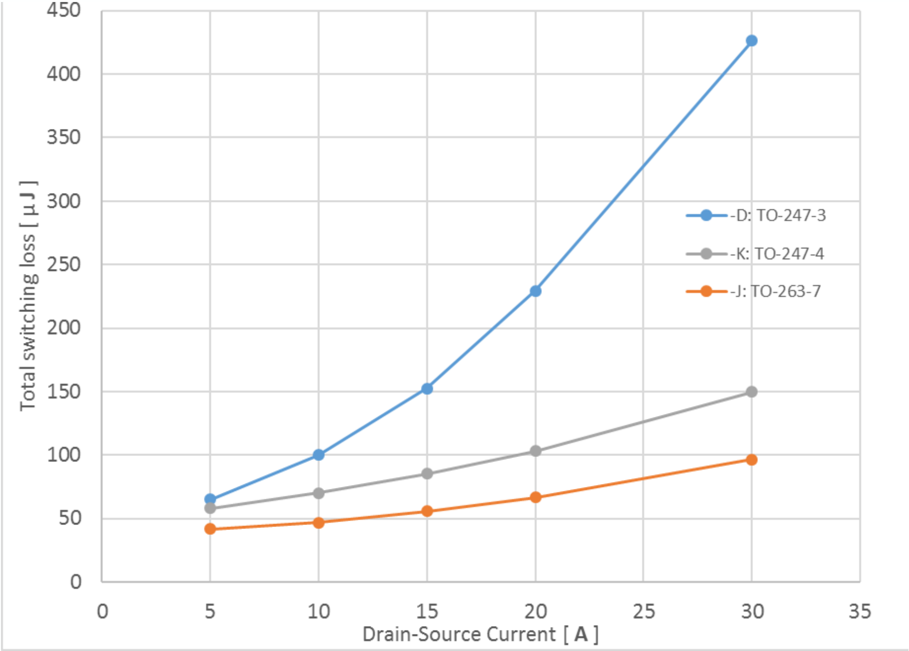
Why SiC?

- ➢ **Fast switching and low switching losses**
- ➢ **Less temperature dependence of Rdson and low conduction loss at high temperature**
- ➢ **Low reverse recovery body diode for hard-commutation**

  - ✓ **Enabling higher switching frequency**
  - ✓ **Increasing power density and reducing weight**
  - ✓ **High efficiency**
  - ✓ **Bi-directional operation**

Package Selection

Switching Loss Comparison @ Exactly Same Test Conditions



TO-247-3
NO - Kelvin Pin
2.6mm Creepage
8nH Inductance

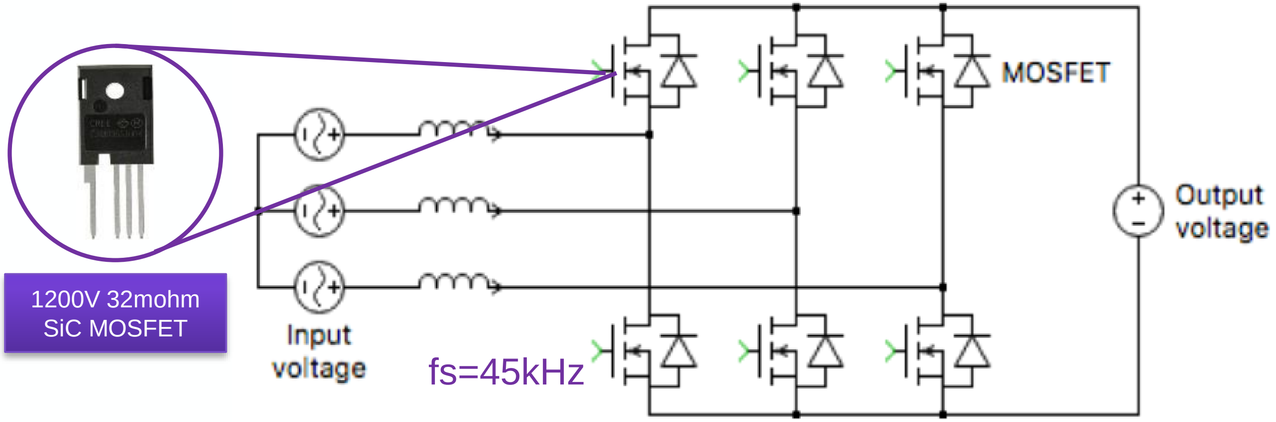
TO-247-4
Kelvin Pin
8mm Creepage
8nH Inductance

TO-263-7
Kelvin Pin
7mm Creepage
2nH Inductance

✓ TO-247-4 package is selected for efficiency, reliability and thermal management.

Power Components Selection

The DC link voltage is up to 900V.



C3M0032120K 1200V 32mohm SiC MOSFET is selected for AFE based on electrical stress and thermal design.

- ❑Best figure of merit (FOM)
- ❑New K-Source package reduces switching loss and reduce cross talk
- ❑Easy to drive (V_{gs} = +15V)

Key Magnetics Design

Parameters and Performance Comparison– Power Choke

	APH	NPH	NPH-L	NPA	KAM
ui	60	60	60	19/60	60
Pv(100mT @50kHz)	250kW/m3	260kW/m3	200kW/m3	100kW/m3	200kW/m3
DC Bias (@100 Oe)	73%	61%	58%	55%	68%
Frequency Range	<200kHz	<200kHz	<200kHz	<300kHz	<300kHz
Vendor	AMOGREENTECH	POCO	POCO	POCO	KDM

- ✓ KAM material is selected for PFC choke. It is a trade-off between core loss and DC bias.
- ✓ NPA material is selected for resonant chokes due to its lower core loss

Key Magnetics

- PFC Choke:

Option1: KAM250060A 2mm wire*2 40turns

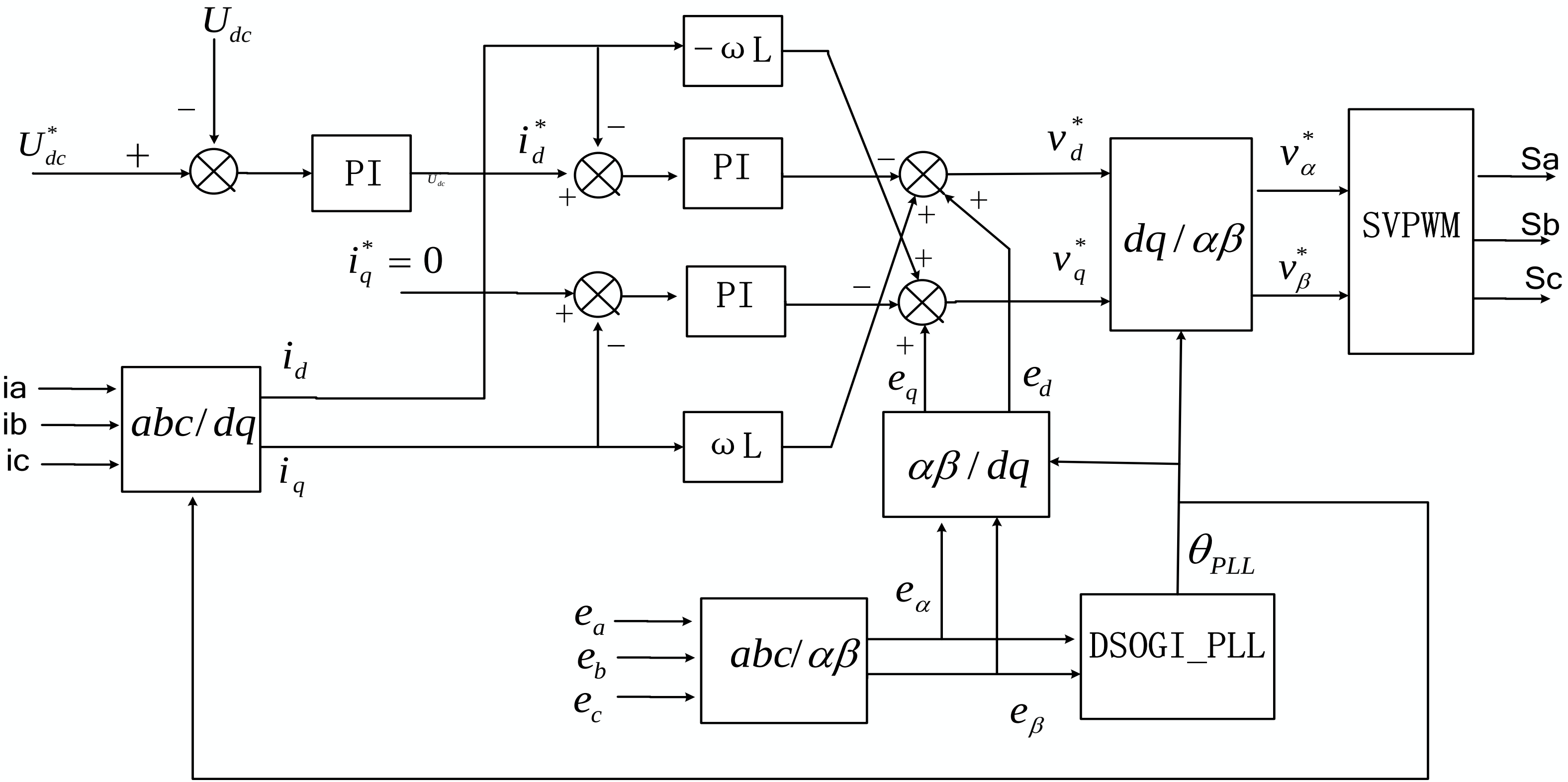
Contact info: Jinbo Cai, Sunlord, jinbo_cai@sunlordinc.com

Option2: NPH250060-L 2mm wire*2 40turns

Contact info: Vivien Luo, POCO, vivien_luo@pocomagnetic.com

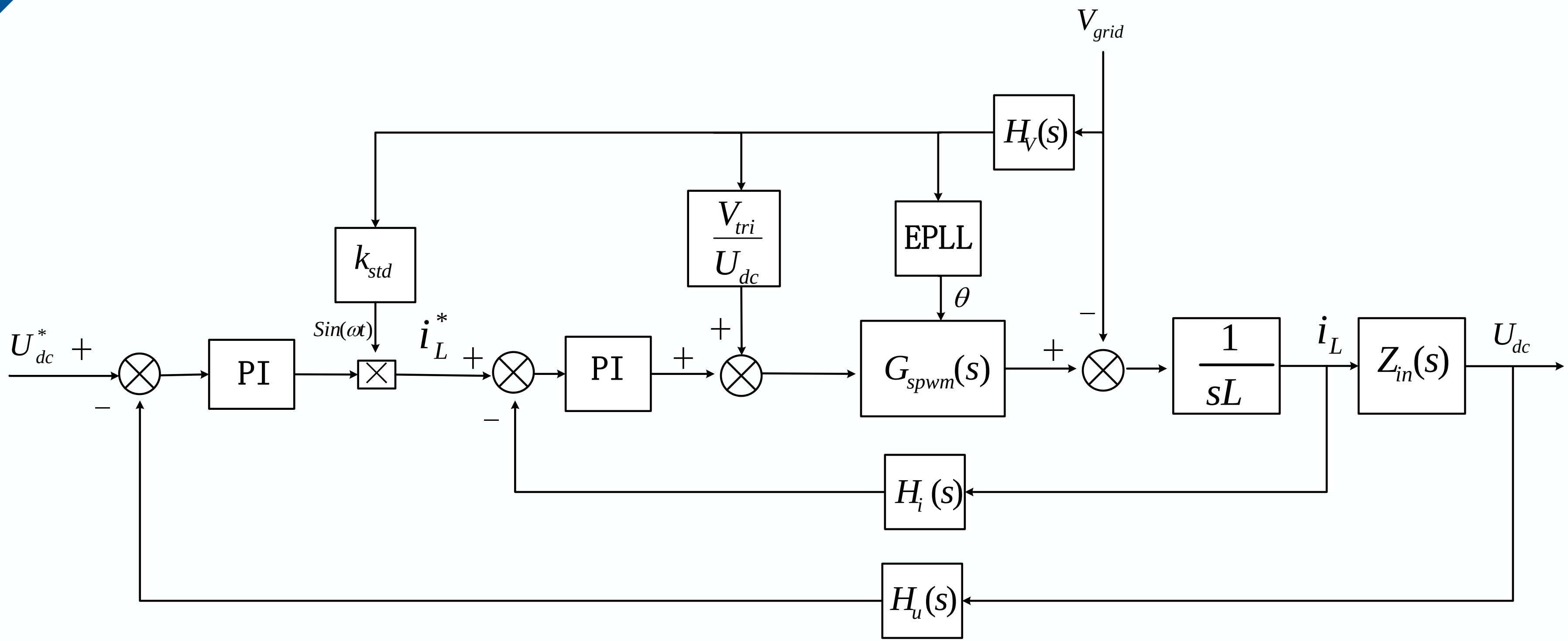
Brief Introduction of the Control

The Control of AFE converter: Three phase mode



Based on TI C2000 duo core DSP TMS320F28377D

The Control of AFE converter: single phase mode



Flexible Digital Control

Single Phase Charging Mode
Bridgeless Totem pole PFC Converter - Average Current Control

According to the direction of input voltage, the phase C bridge as low frequency with alternating conduction. The phase B bridge arm as high frequency switch with complementary conducting. For phase B, the main switching MOSFET and the commutation MOSFET are periodically alternated according to the input voltage. The switching frequency is 45kHz.

Three Phase Charging Mode
Six Switches AFE Converter - SVPWM Control

In the equivalent two-phase static coordinate system, there are eight different combinations of the control signals of each arm switch. Therefore, the space vector of the output voltage of the converter runs as close to the circle as possible. The switching frequency is 45kHz.

Flexible Digital Control

Single Phase Discharging Mode
Interleaving Buck - Open Loop

According to the positive and negative direction of the input voltage, the two-phase bridge arm alternates conduction. Then the high and low switch complementary conduction in each phase. The duty cycle is fixed, and the switching frequency is 45kHz.

Three Phase Discharging Mode
Six Switches AFE Converter – Open Loop

This mode is used for checking driving signal when we power up at the first time. The frequency is 45kHz. This mode can also be used in discharging mode three phase AC output. The output voltage is about 380Vac when the input voltage is 750Vdc.

Gate Driving Voltage V_{GS}

Max Gate Drive Voltage

Maximum Rating Gen3 650V MOSFET

V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 29

V_{GS} maximum rating is -8/19V as shown in the waveform. The positive max V_{GS} rating is 19V. The negative max V_{GS} rating is -8V. The max V_{GS} rating allows for ringing and overshoots that will be superimposed on top of the continuous gate drive voltage. As long as the peak transient voltages don't exceed the part's max V_{GS} rating, the device will run properly and there is no degradation to the device's life or reliability. For negative V_{GS} , the pulse width must be less than 100ns when Vgs <-6V in the transient events.

- Negative Gate-Source bias voltage will ensure MOSFET staying off for half bridge topology to avoid parasitic turn-on due to cross talk.
- +15V/-3V is recommended. The users can choose turn-off voltage range -2V~ -4V.

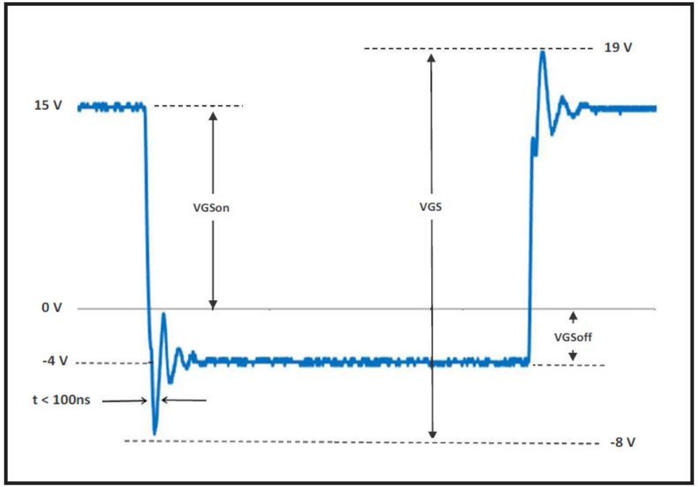
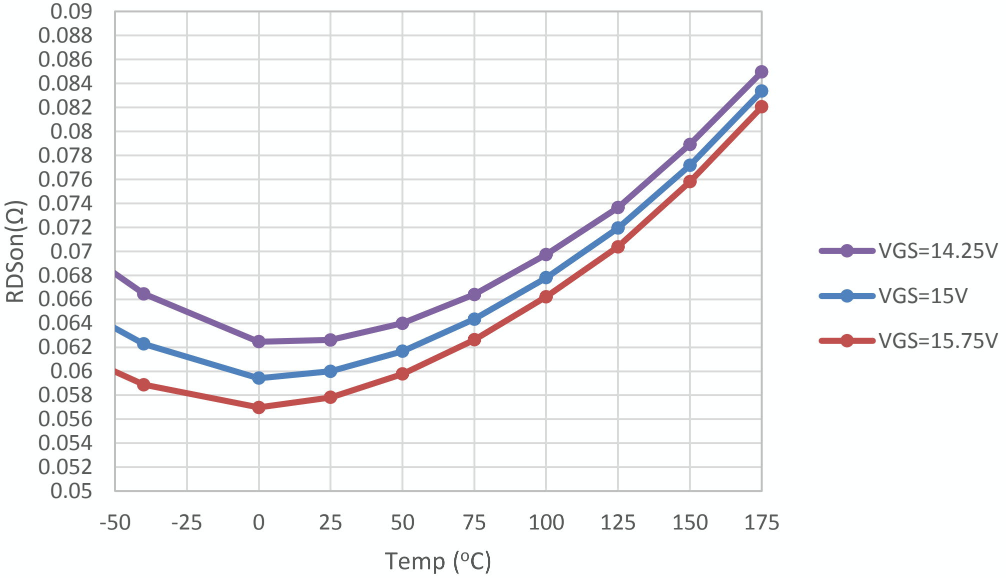


Fig. 29

Rdson under Turn-on Voltage Tolerance C3M0060065K testing

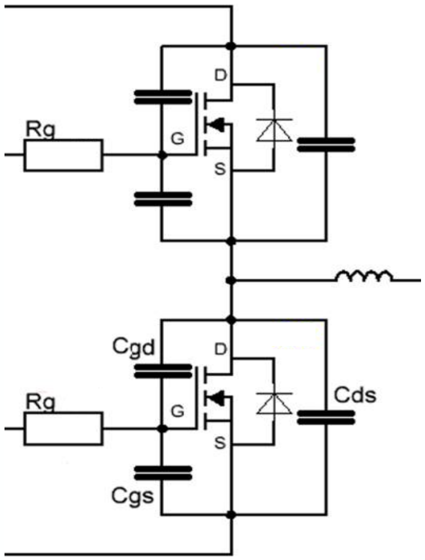


In practical design, power supply tolerance must be considered. The guidance is within +/-5% tolerance.

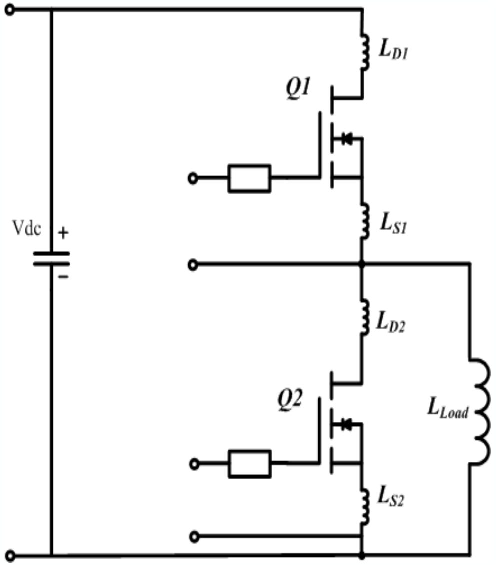
The impact of Rdson due to V_{GS} variation. Rule of thumb, the 5% of gate voltage tolerance will cause around 4% Rdson variation at 25ºC and 2% variation at 125 ºC.

Why Negative Voltage Is Required in Half Bridge?

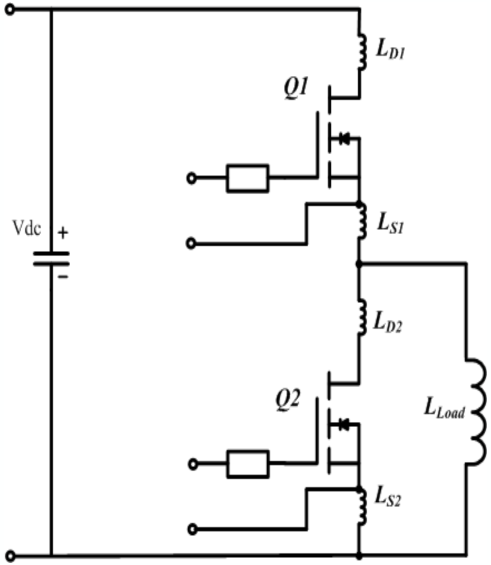
Cross Talk in Totem Pole Half Bridge (Totem Pole)



Switch without package parasitic

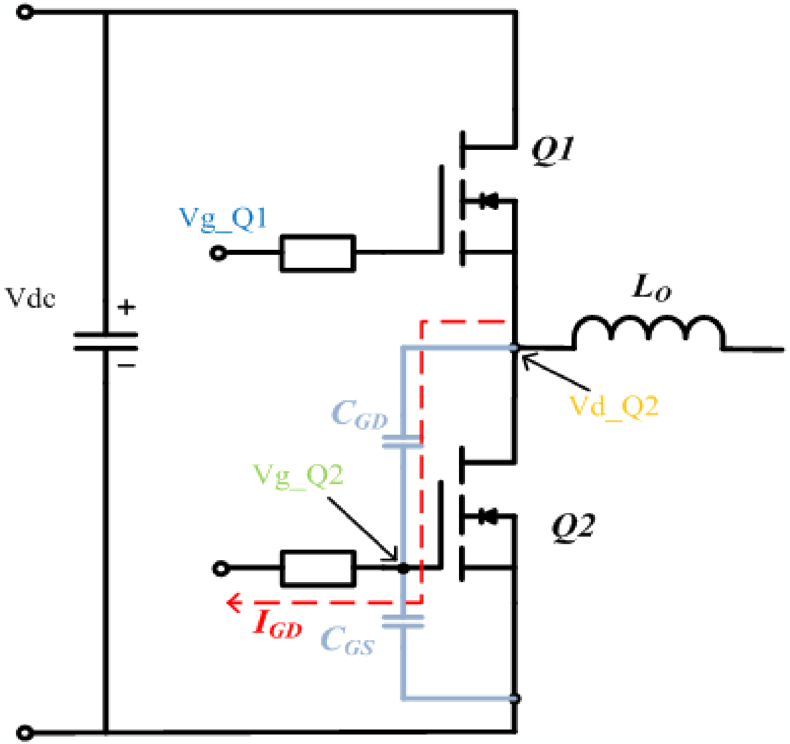


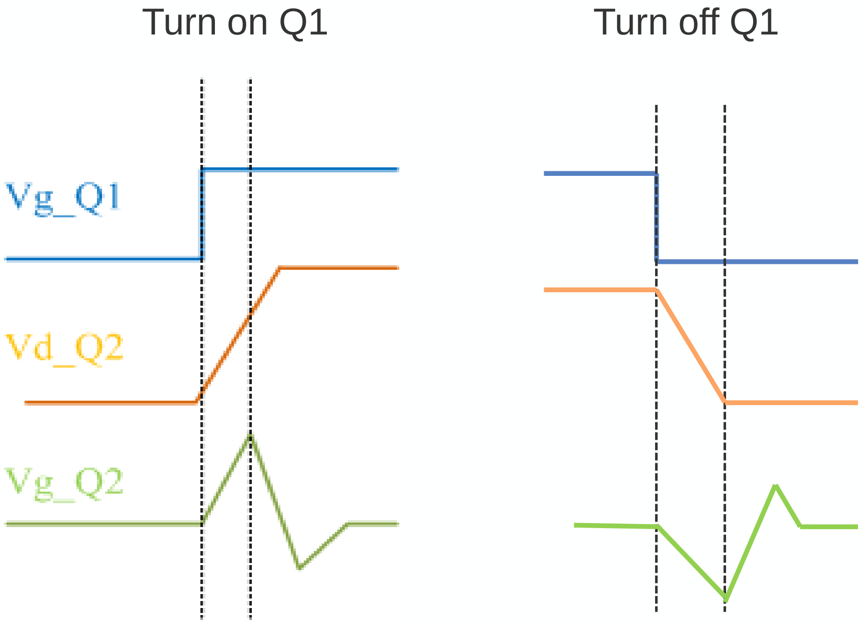
3L package



4L package

Cross Talk in Ideal Totem Half Bridge by dv/dt Only





If dv/dt=100V/ns, and C_{GD}=10pF

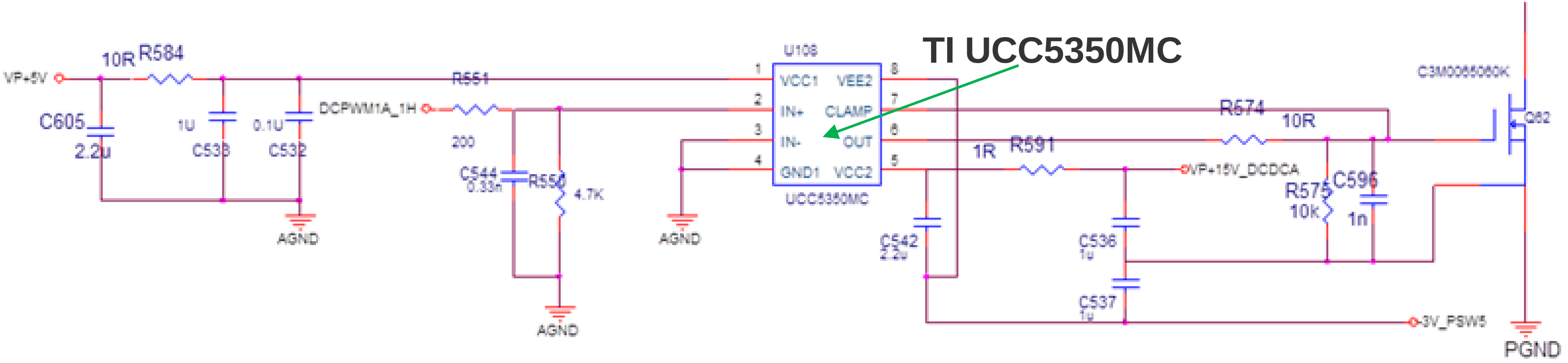
I_{GD} ~ C_{GD} * dv/dt=1A

Vgs_spike ~ Rg* I_{GD}

Gate Driver and Bias Power Supply

Tips for SiC MOSFET Gate Driver Circuit

- CMTI (>100KV/us)
- VIORM Maximum Working Insulation Voltage
- Driving capability
- Propagation delay time (~50nS) and channel mismatch time (~10nS)
- Active miller clamp
- Additional cap or RC from Gate to Kelvin Source

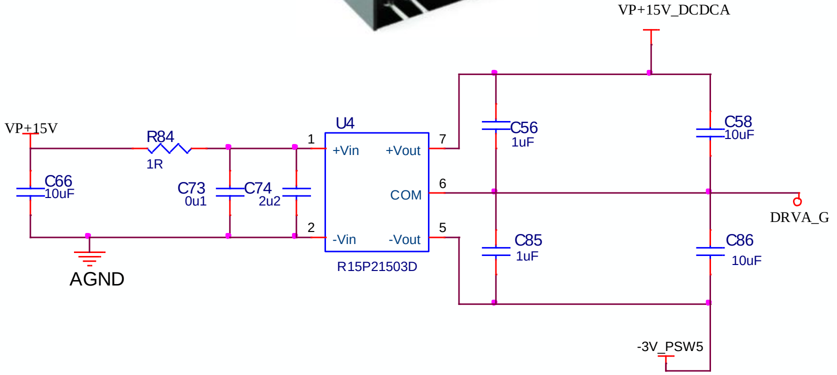


How to Generate Bias Voltage? Option 1

Dedicated +15V/-3V power supply

Wolfspeed has worked with partners (RECOM, MOURSUN) to make power modules

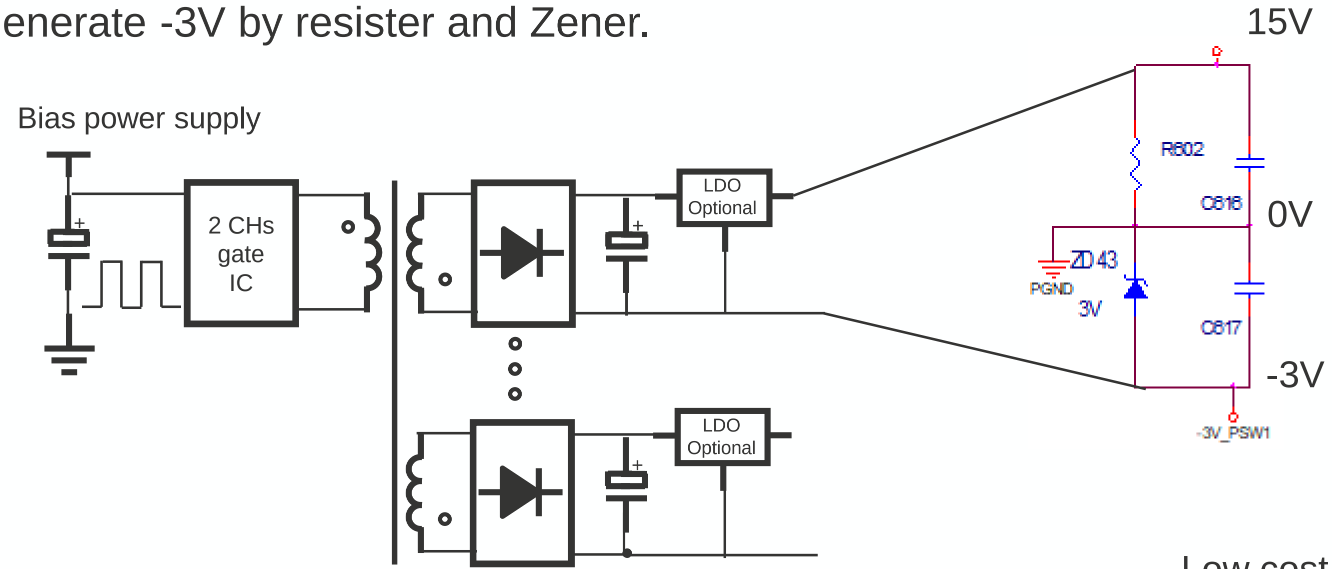
- RECOM R15P21503D and R12P21503D
- MOURSUN QA15115R2



Easy to use

How to Generate Bias Voltage? Option 2

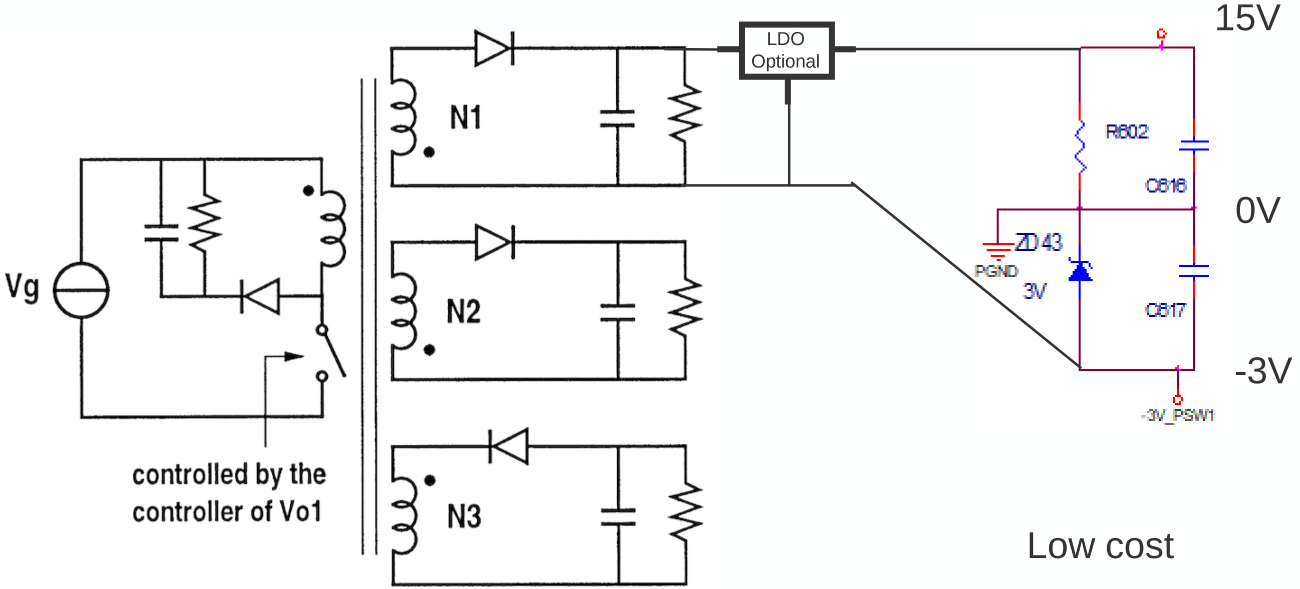
- Open loop controlled 18V multi-outputs Aux power supply based on bias power supply of the system.
- Generate -3V by resister and Zener.



Low cost

How to Generate Bias Voltage? Option 3

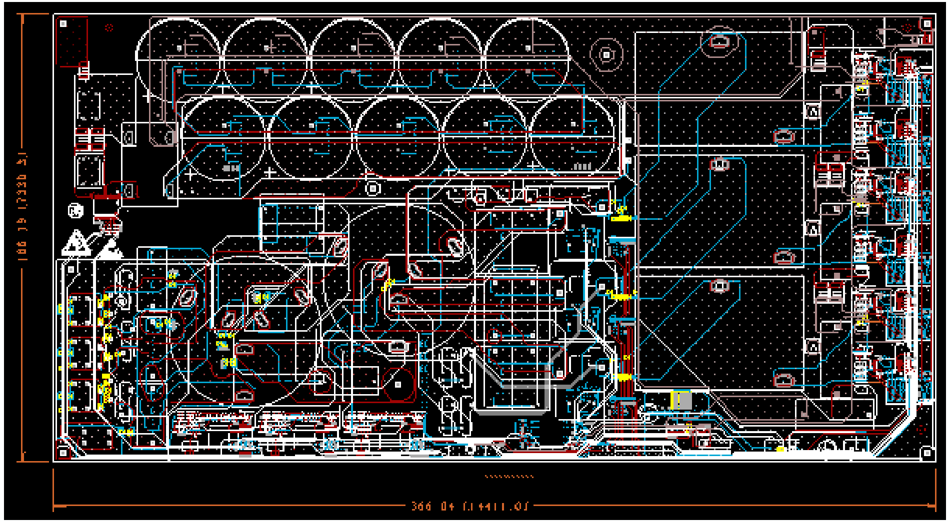
- Closed loop controlled 18V multi-outputs flyback converter.
- Generate -3V by resister and Zener.

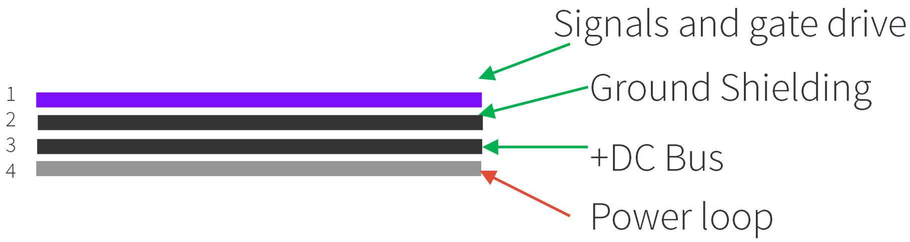


Low cost

PCB Layout Considerations

4layers Power Board

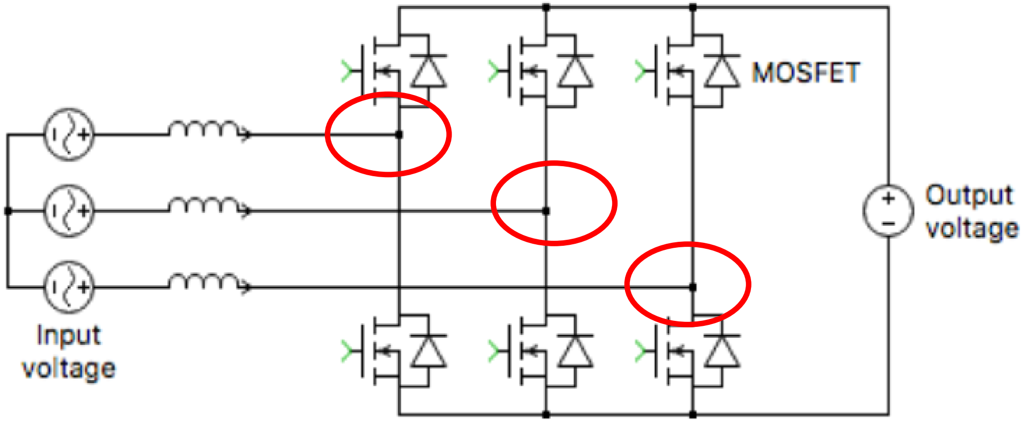




Tips(for 4layers PCB):

- No overlap between sensitive signals and the power loop.
- 2nd layer for GND. The ground layer acts as a shielding to cover the signal traces and gate drive circuit at the 1st layer.

High dv/dt trace/node



- Keep the sensitive signals far away from the high dV/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as resonant choke, power transformer.
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance

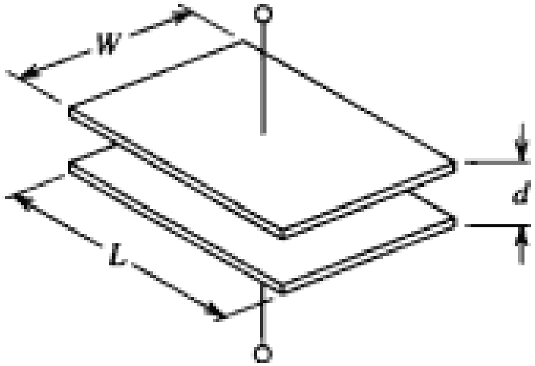
Parasitic Caps of PCB

$C = \varepsilon_r S / 4\pi k d$

$1/4\pi k = 8.85\times10^{-12}$F/m

ε_r of FR4 →~4.3

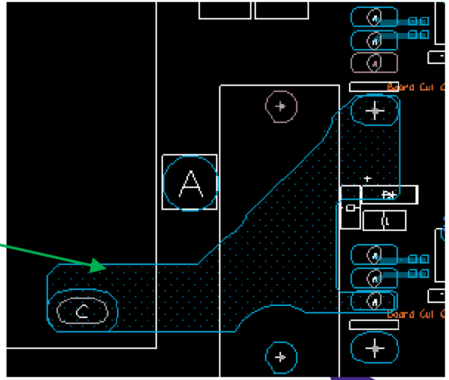
d = 0.0001m



For 1 cm ^{2} PCB trace overlap:

$C = 4.3*0.01*0.01*8.85\times10^{-12} / 0.0001 = 38$pF

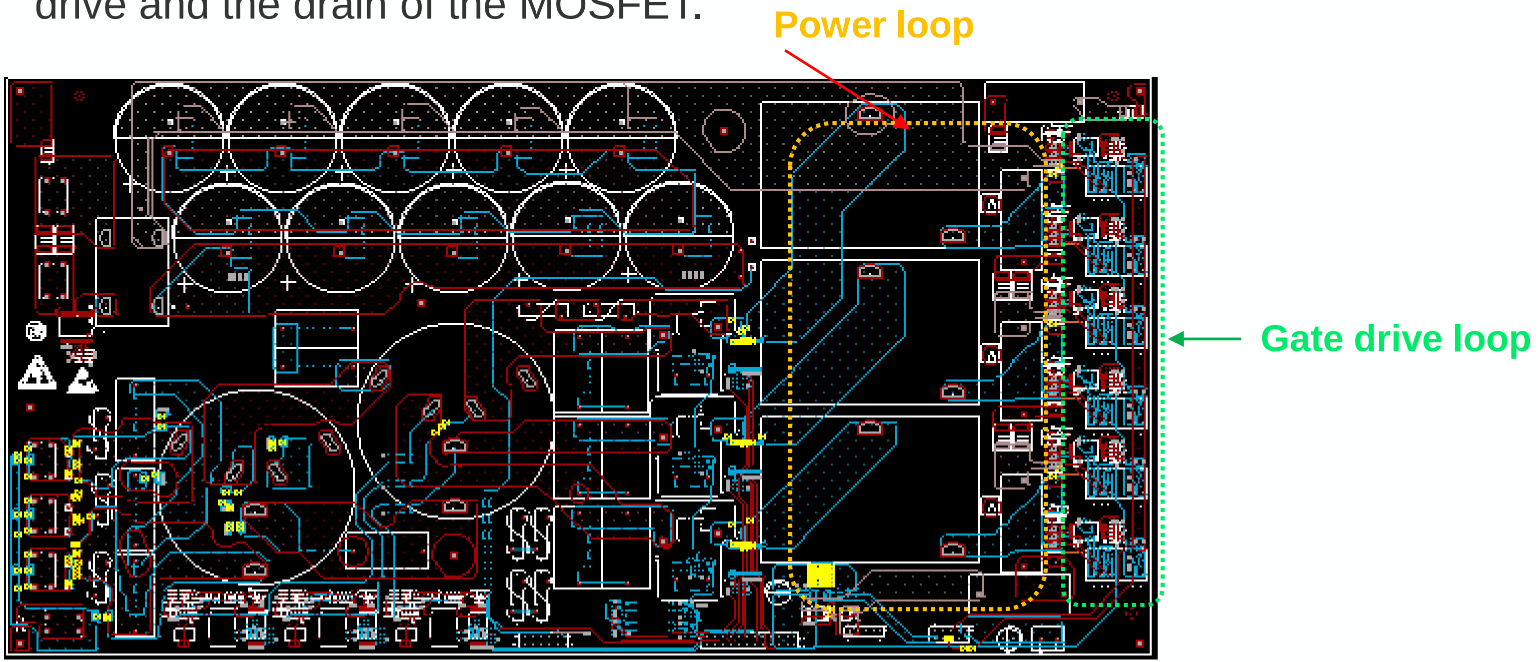
$P_c = 0.5*C*f*V^2 =$ 1.2W for 800Vbus hard switching @100kHz



- Short and small traces to reduce the coupling and parasitic capacitance.

Components Placement

- Avoid overlap between Gate, Gate drive circuit, bias power supply for Gate drive and the drain of the MOSFET.

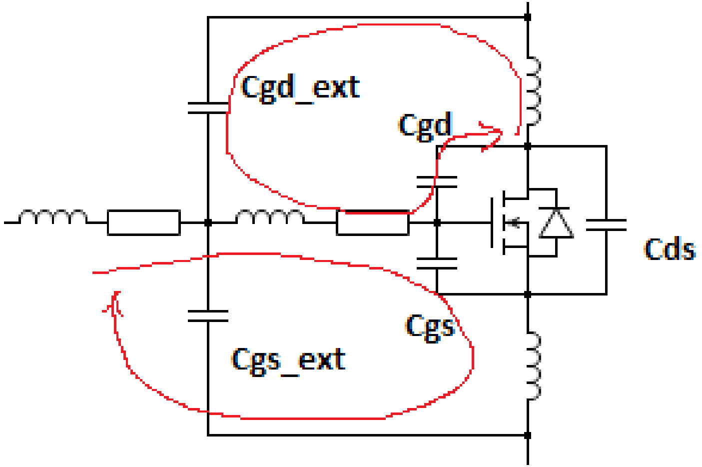


Impact due to the external parasitic cap

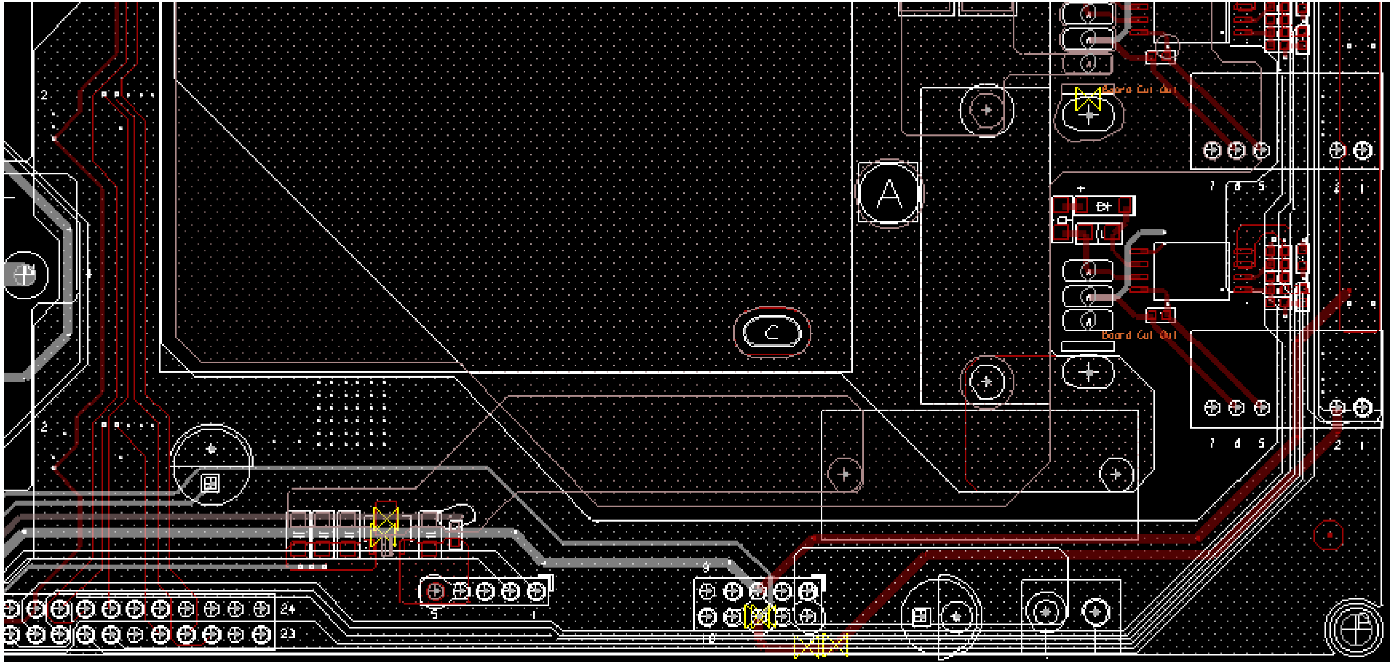
Impact due to the parasitic cap by overlap between drain and Gate + Gate drive circuit.

1. Switching loss increased due the larger total Qgd
2. Enhanced cross-talk due to the larger ratio between Cgd and Cgs. →shoot through and higher voltage spike.
3. Cgd_ext can even enhance the gate oscillation. → impact the reliability

$I_D = (V_{GS} - V_{TH}) * g_{fs}$

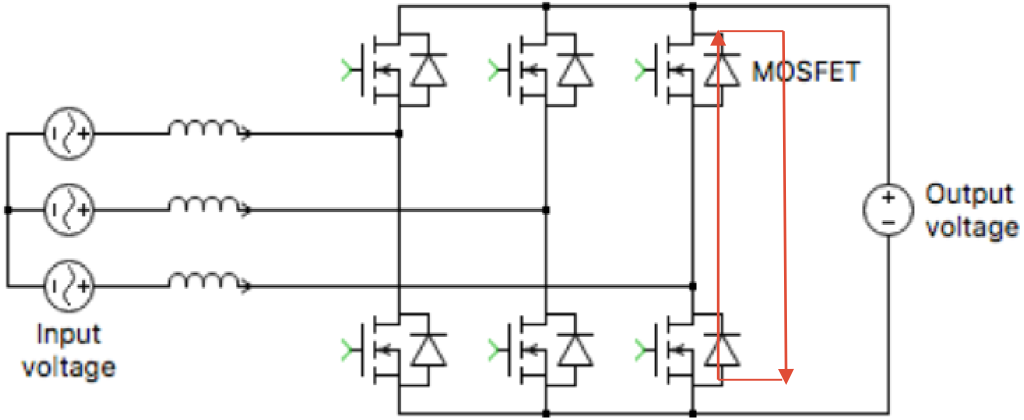


Sensitive Signals



- Keep the sensitive signals far away from the high dV/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as PFC choke, DCDC power magnetics.
- Route them at edge or the power board or other “clean” areas.
- Covered by ground shielding.

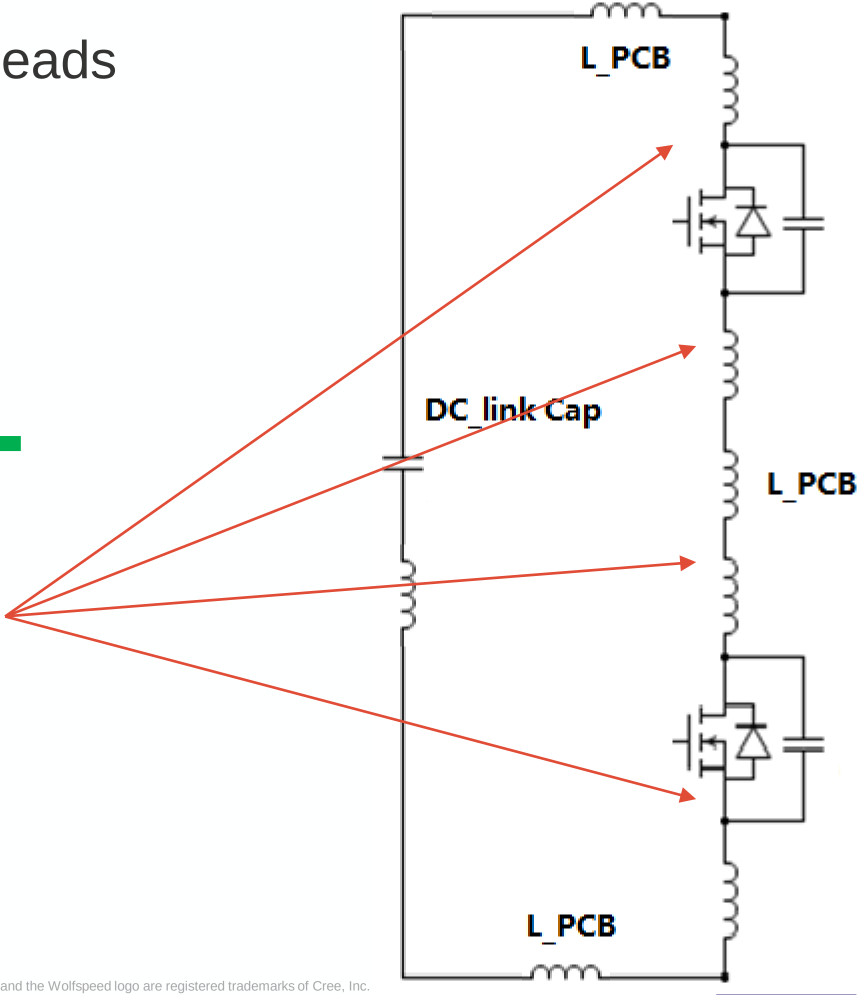
High di/dt loop



•Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
•Proper PCB layout of the power components to minimize the high frequency di/dt loop.

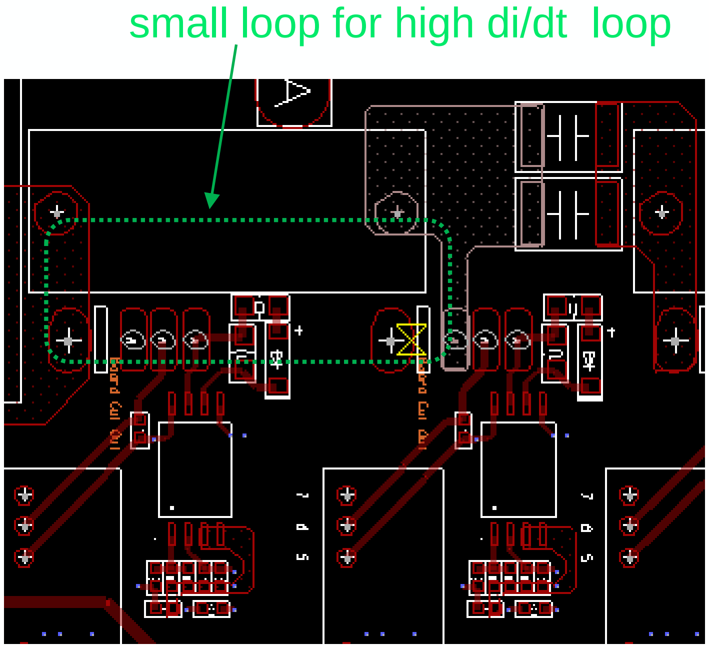
Parasitic Inductance of PCB and leads

or



- Long lead/trace introduces drain voltage spike due to parasitic inductance.
- Long lead/trace introduces gate voltage oscillation.

High di/dt loop

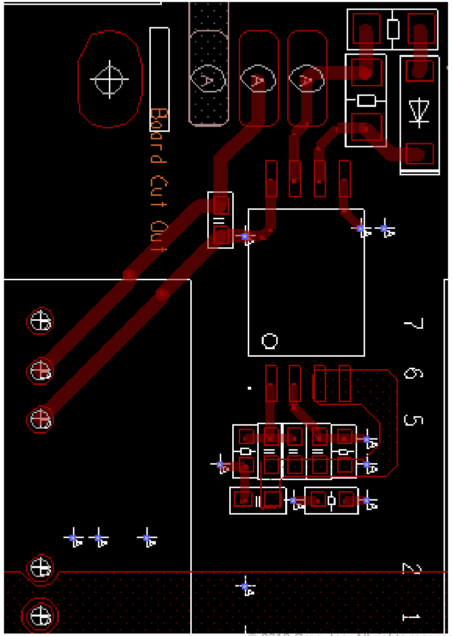


•Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
•Proper PCB layout of the power components to minimize the high frequency di/dt loop.

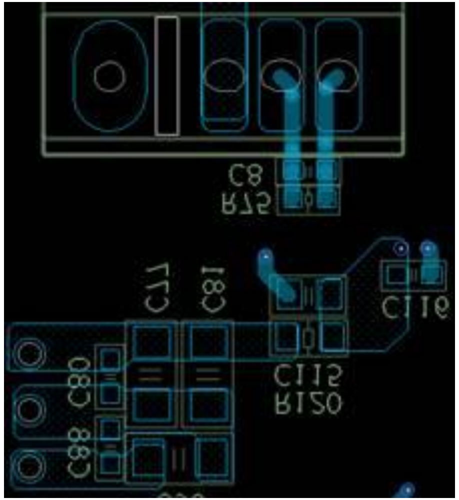
SiC MOSFET Gate Driver

- Minimized the loop of gate drive
- Minimized the loop of active miller clamp
- Separated gate source. Don’t introduce parasitic inductance from power source loop
- Place the external Gate to Source cap as close as possible to the MOSFET

top



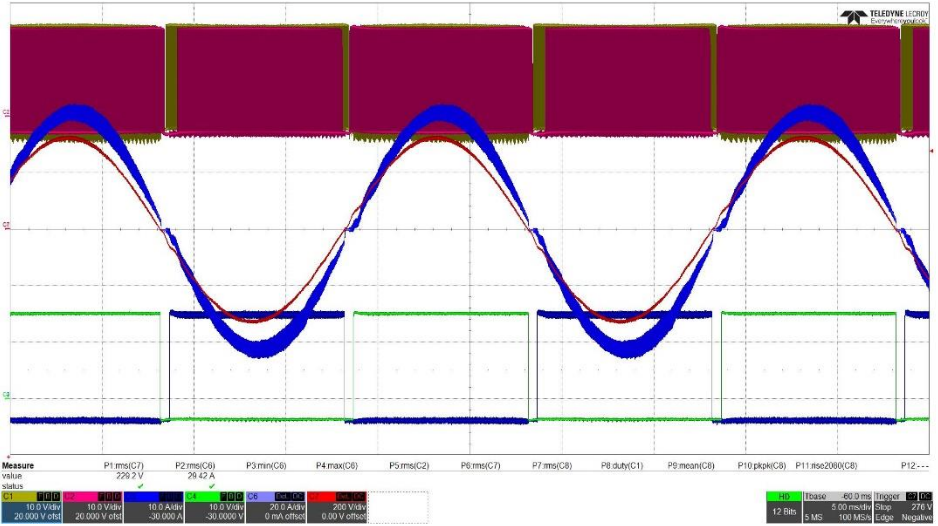
bottom



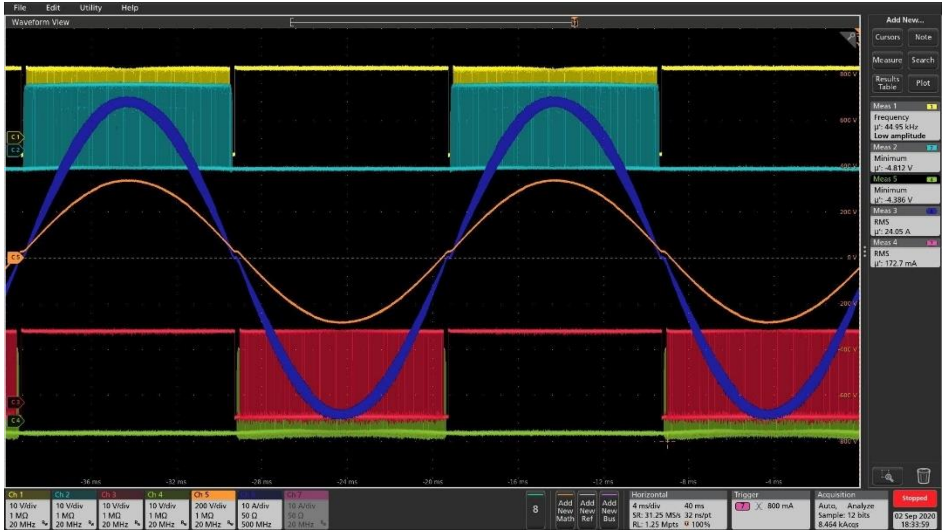
Test Results

Test Result ACDC Waveforms @ Single phase AC

Charging Mode



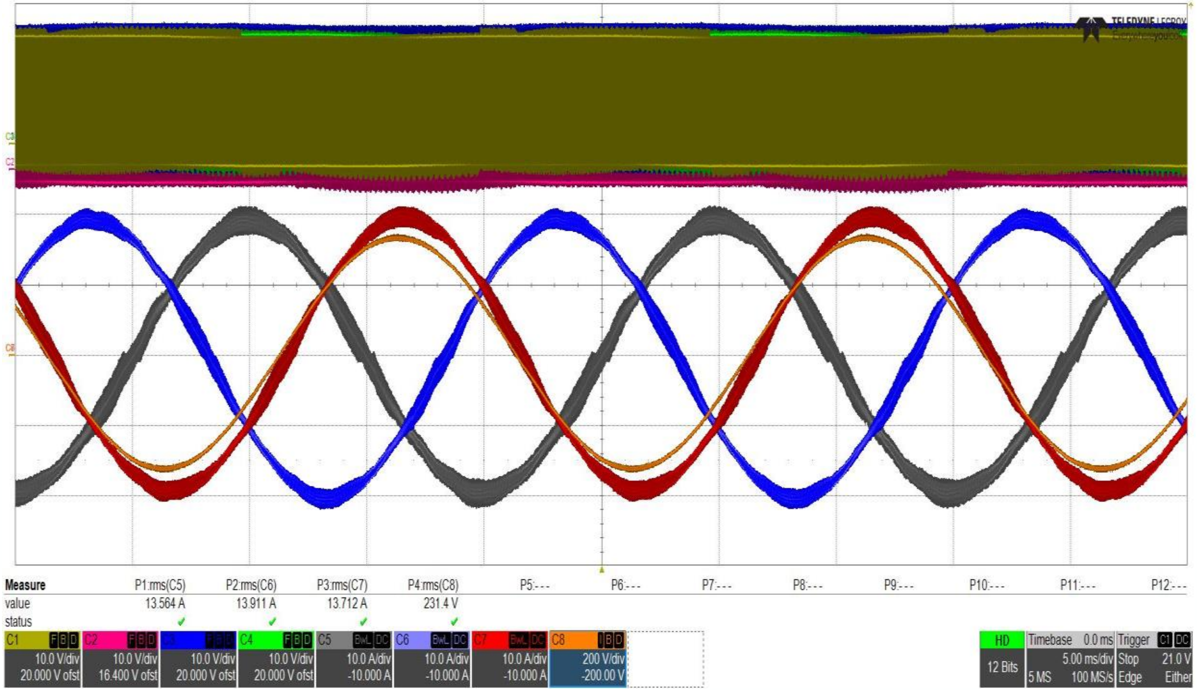
Discharging Mode



CH1: Vgs high frequency, high side
CH2: Vgs high frequency, low side
CH3: Vgs low frequency, high side
CH4: Vgs low frequency, low side
CH6: Choke current of LB
CH7: Input voltage

CH1: Vgs B phase Low side
CH2: Vgs B phase High side
CH3: Vgs C phase Low side
CH4: Vgs C phase High side
CH6: PFC choke current
CH7: Output Voltage

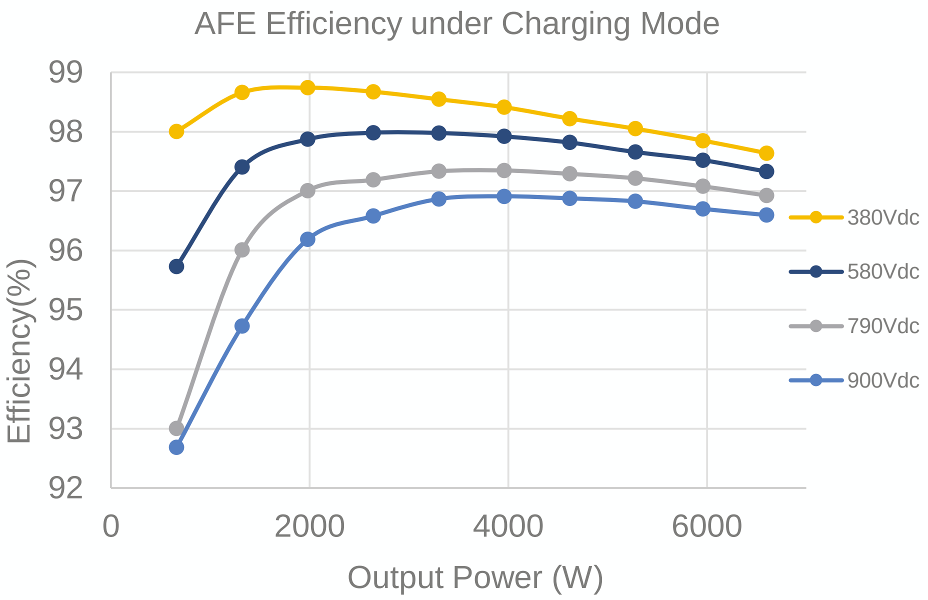
Test Result ACDC Waveforms @ 3 phase AC



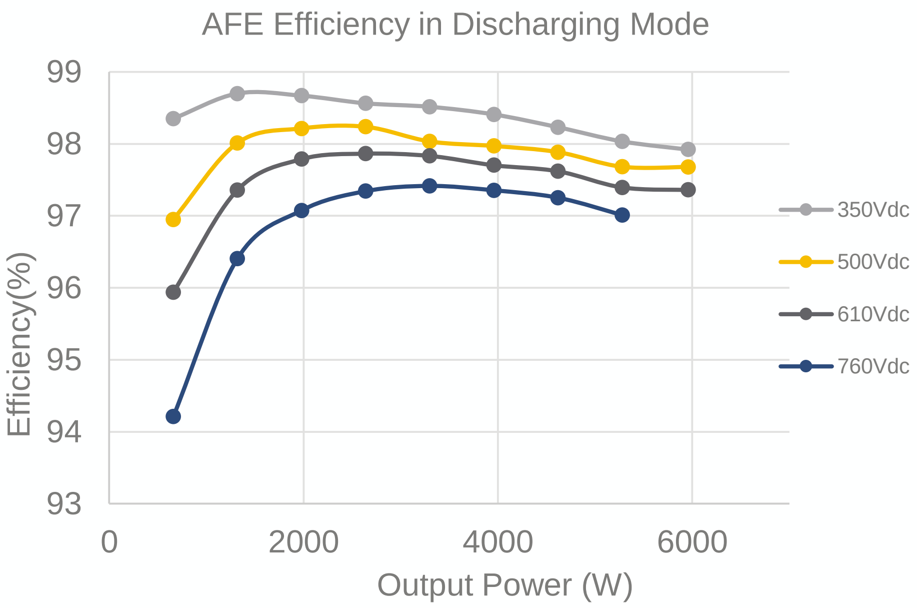
CH1/3/4: Vgs low side of phase C/B/A
CH2: Vgs high side of phase B
CH5-7: Choke current of LA、LC、LB
CH8: Input voltage of phase B

Test Result Efficiency @ Single phase AC

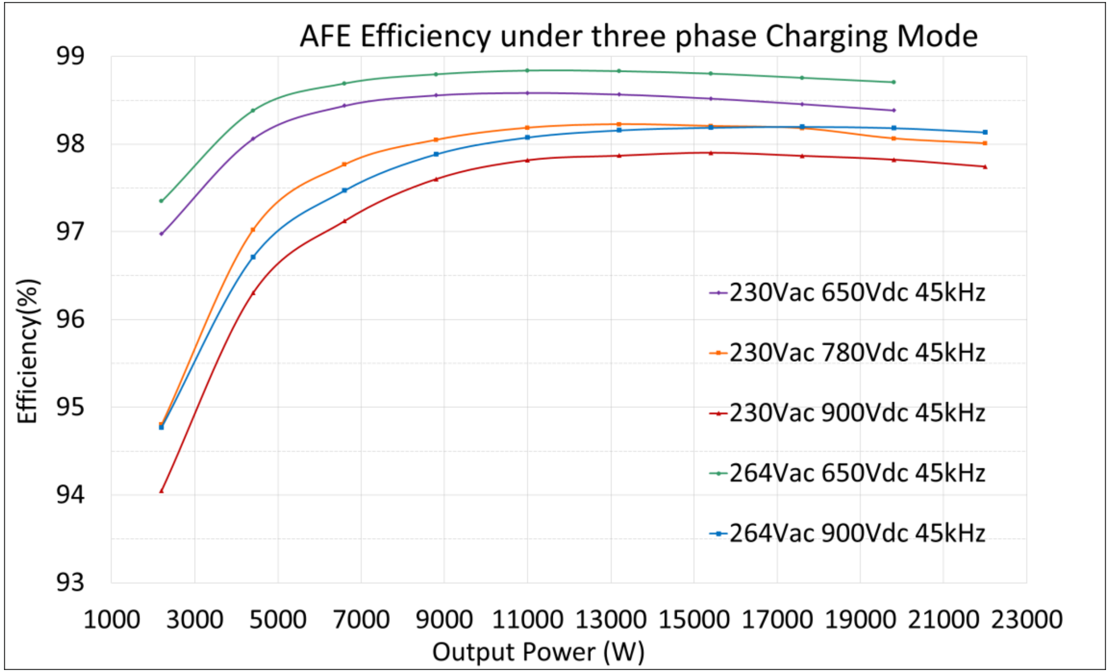
Charging Mode



Discharging Mode



Test Result Efficiency @ 3 phase AC Charging



Thermal Analysis

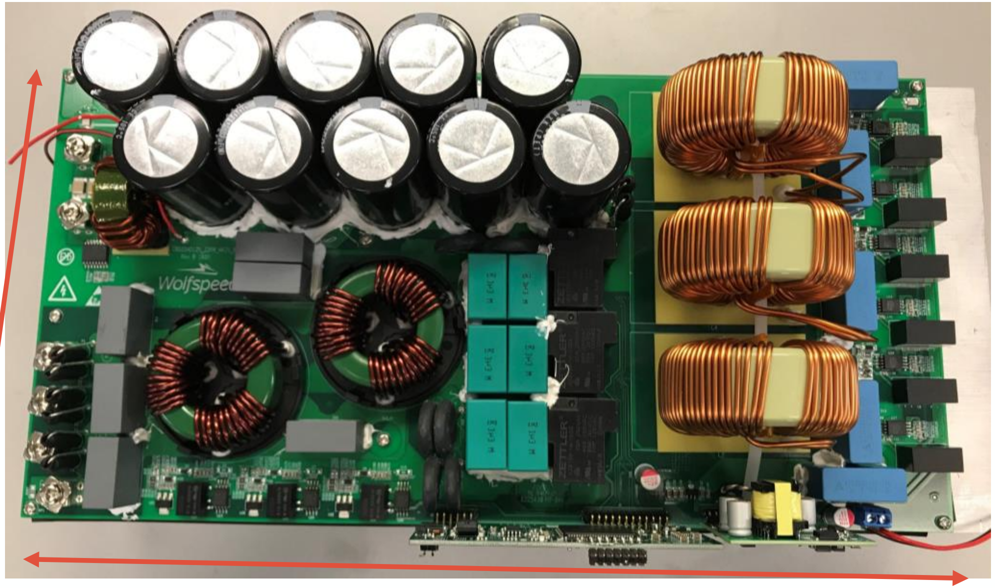
Description	Rth (j-c) (c/w)	Calculated Power Loss (watts)	Case Temp.	Calculated Junction Temp.	Max. Operating Junction Temp.	Comments
Input 380Vac Output = 900Vdc 22kW						
PFC MOSFET	0.45	52	89.4	112.4	175 °C	**PASS**
Input 215Vac Output = 900Vdc 6.6kW						
PFC MOSFET HF	0.45	42	84.9	103.9	175 °C	**PASS**
PFC MOSFET LF	0.45	20	69.1	78.1	175 °C	**PASS**
Input 760Vdc Output 220Vac 6.6kW						
PFC MOSFET	0.45	36	79.8	96.1	175 °C	**PASS**

- $T_{base\ plate}$=65°C

Chen Wei

Picture of the hardware

186mm



366mm

PCBA Dimensions	366mmx186mmx70mm

Design Support Document

Block Diagram | Documentation

Filter by: Document Type

Document Type	Document Name	Version	Date Updated	Download
Application Notes	CRD-22AD12N User Guide		Feb 4, 2021	
Design Files	CRD-22AD12N ALL Design Files		Feb 4, 2021	
Design Files	CRD-22AD12N BOM		Feb 4, 2021	
Design Files	CRD-22AD12N Magnetics Specs		Feb 4, 2021	
Design Files	CRD-22AD12N PCB		Feb 4, 2021	
Design Files	CRD-22AD12N Schematics		Feb 4, 2021	
Design Files	CRD-22AD12N Training Presentation		Feb 4, 2021	

Firmware request online

Applications

- EV On-Board Charger
- EV Off-Board Fast Charging
- Industrial Fast Charging
- Energy Storage Systems

What's Included

- Reference Design Files for
  - Main Board
  - Controller Board
  - Aux Power Board

Request Separately

- Compatible bi-directional DC/DC converter CRD-22DD12N
- Firmware and GUI
- Mechanical Specifications
- Request Firmware

Product Compatibility

- C3M0032120K

Block Diagram | Documentation

Summary

This 22kW AC/DC design demonstrates performance of Wolfspeed Gen3 1200V SiC MOSFET for three phase AFE for OBC, fast charger, ESS, etc .

- ✓ High Efficiency > 98.5% in charging and discharging mode
- ✓ Bi-directional Operation
- ✓ Support both 3phase AC and single AC input
- ✓ Support 380Vdc-900Vdc wide DC-link voltage range